Flexus CMP Coherence Protocol

- Notation

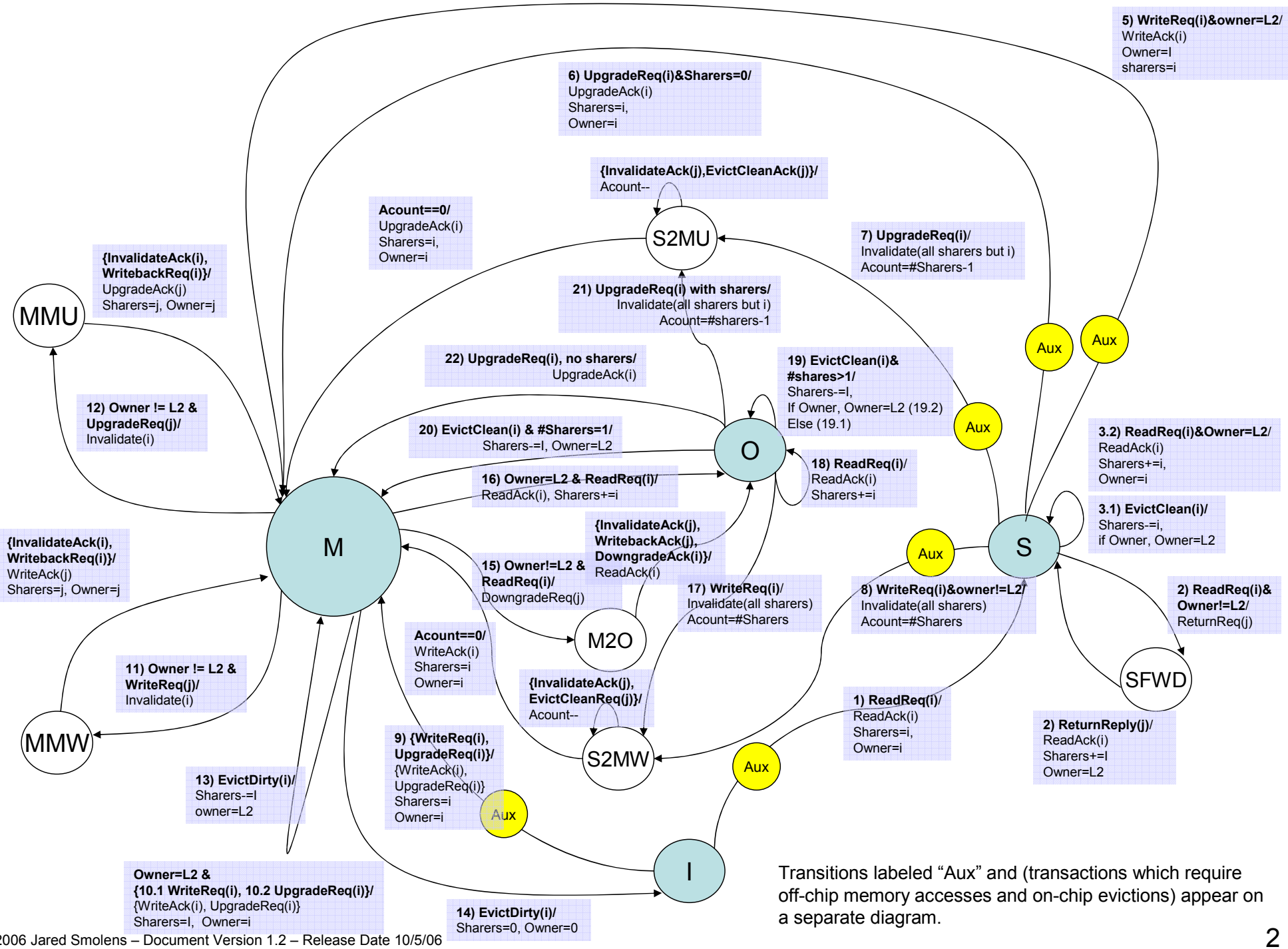
  Message_received, transition_guard_conditions/
  Messages_sent, state_update_actions

- State maintained per cache line at CMP directory
  - Protocol state: tracks stable and transition states in CMP
  - Sharers bit vector: tracks on-chip sharers
  - Owner field: specifies who is responsible for the **last copy** of the line within the CMP (L2 if owned by shared cache)
  - Additional temporary data for handling transient states

- As in Piranha CMP protocol, blocks allocated directly in L1s
  - Shared cache acts as a large victim cache for L1 replacements
  - Both clean and dirty blocks written back to L2 by owner

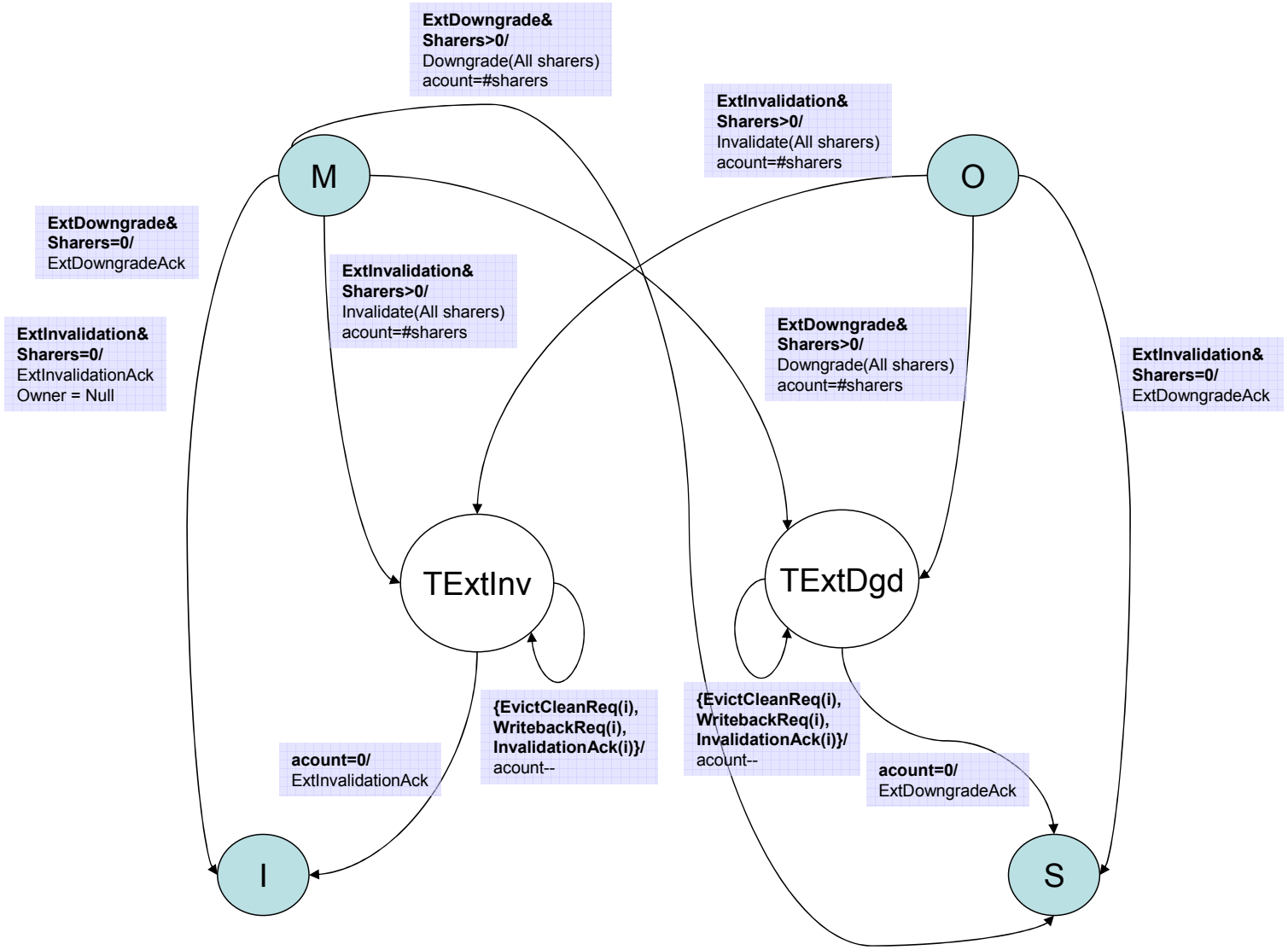
- References
  - Piranha: A Scalable Architecture Based on Single-Chip Multiprocessing, ISCA'00

Flexus CMP Coherence Protocol



Transitions labeled “Aux” and (transactions which require off-chip memory accesses and on-chip evictions) appear on a separate diagram.

Flexus CMP Coherence Protocol – Responses to External Messages (from off-chip)



Flexus CMP Coherence Protocol – Aux Requests and Evictions
Aux requests handle off-chip misses