CS-206 HW1

Basic Architecture

25 Feb 2015

Deadline: 03.03.2015
Submission: Please make a PDF file of your answer and upload it in the moodle using related box. Do not forget to write your Name and Sciper number.
Please write clearly and concisely.

1. You are given the following four options to change cache miss rate (Each option is applied alone, without changing the other parameters):

   A. Change cache size
   B. Change block size
   C. Change associativity
   D. Prefetch next-block

   Which of the above options have effect on:

   I. Compulsory misses:
   II. Capacity misses:
   III. Conflict misses:
   IV. Coherence misses:

   Describe the effects of the changes.

2. Assume the following code. It is written in C, where elements within the same array are stored contiguously. A and B are two integer arrays (The size of integer is 32 bits). The physical address of A, B and i are 0X0000, 0X1000, 0X2000 respectively.

```
for (i = 0; i<8000; i++)
     A[i] = B[i] + 4;
```

   Assume a cache with the following information:

   - Size: 4KB
   - Block size: 16B
   - Associativity: 4-way
   - Replacement policy: LRU

   a. How many 32-bit integers can be stored in a block?
   b. If this code is executed by a single core, calculate the miss rate.
   c. We divide this code between two cores (each core has its own cache). Core1 is responsible for even indexes and core2 is responsible for odd indexes. Write the code for each core. In this case, calculate the miss rate.
   d. Rewrite the program for two cores to avoid unnecessary misses.